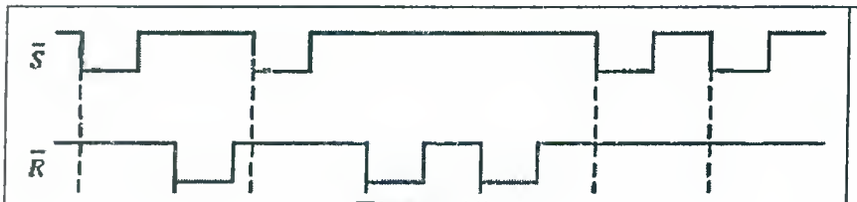
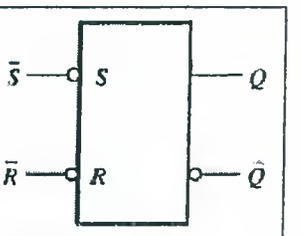
Mansoura University	Logic Circuits 2
Faculty of Engineering	2nd year Students
Communications and Elect. Dept	Time 3 Hours

Q1: If the $\bar{S}$ and $\bar{R}$ waveforms in Figure 1 are applied to the inputs of the latch in Figure 2, determine the waveform that will be observed on the Q output. Assume that Q is initially low.

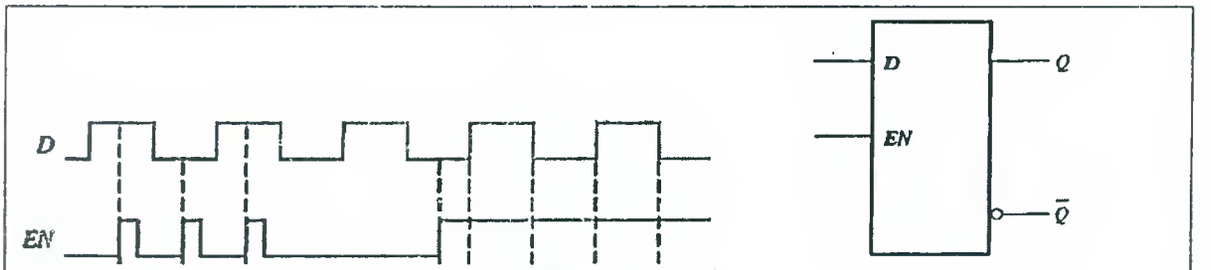


Figure(1)



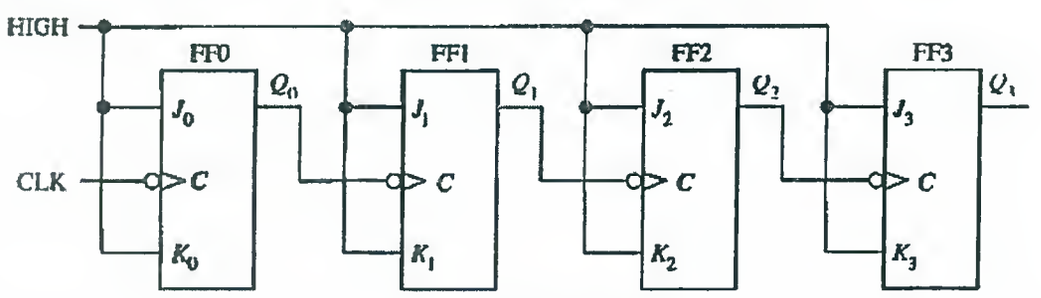
Figure(2)

Q2: Determine the Q output waveform if the inputs shown in Figure 3 are applied to a gated D latch. which is initially RESET.



Figure(3)

Q3: A 4-bit asynchronous binary counter is shown in Figure 4. Each flip-flop is negative edge-triggered and has a propagation delay for 10 nanoseconds (ns). Develop a timing diagram showing the Q output of each flip-flop, and determine the total propagation delay time from the triggering edge of a clock pulse until a corresponding change can occur in the state of Q_3 Also determine the maximum clock frequency at which the counter can be operated.



Figure(4)

Q4: Show the timing diagram and determine the sequence of a 4-bit synchronous binary up/down counter if the clock and UP/DOWN control inputs

have waveforms as shown in Figure 5. The counter starts in the all 0s state and is positive edge-triggered.

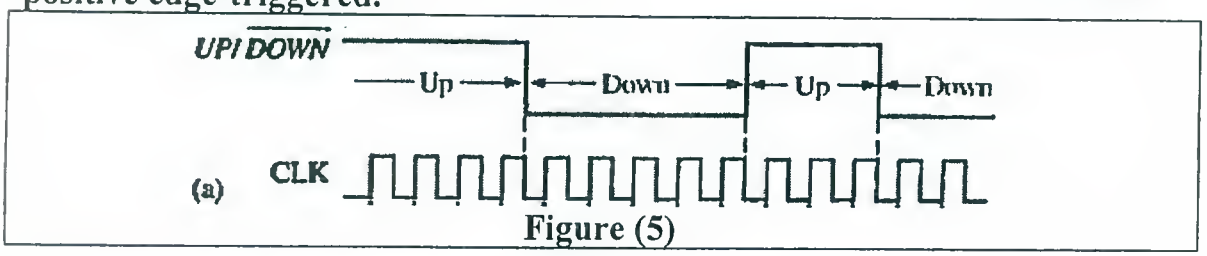


Figure (5)

Q5: Implement the decoding of binary state 2 and binary state 7 of a 3-bit synchronous counter. Show the entire counter timing diagram and the output waveforms of the decoding gates. Binary 2 = $\overline{Q_2}Q_1\overline{Q_0}$ and binary 7 = $Q_2Q_1Q_0$.

Q6: Show the states of the 5-bit register in Figure (6a) for the specified data input and clock waveforms shown in Figure (6b). Assume that the register is initially cleared (all 0s).

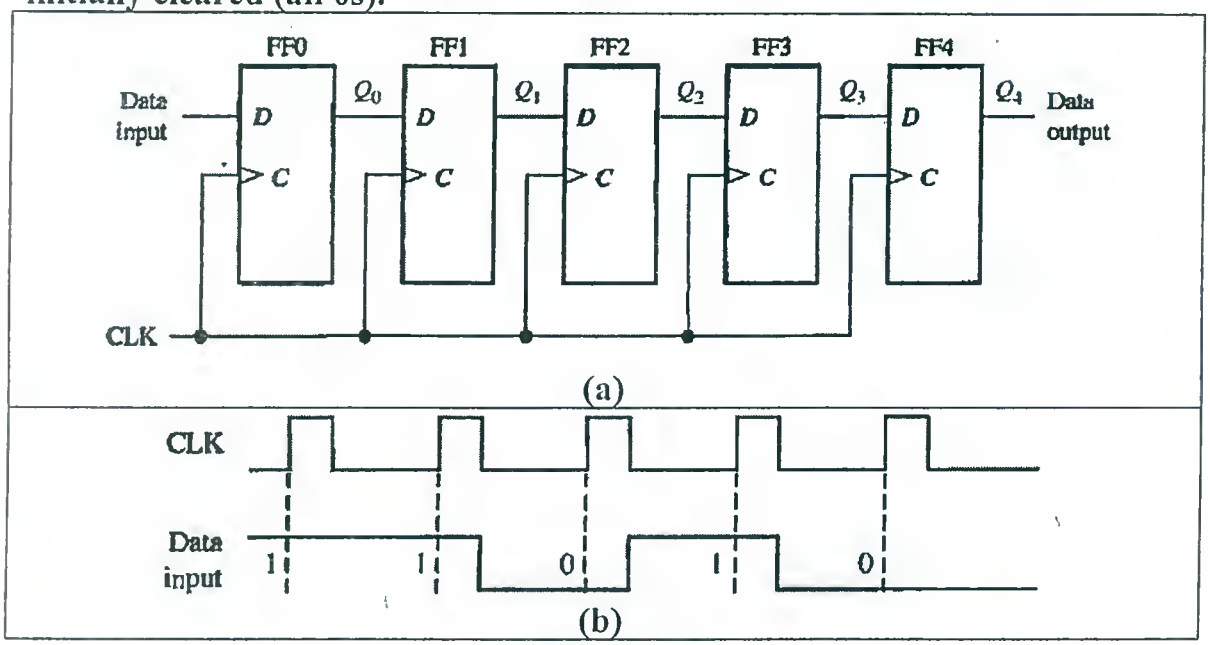
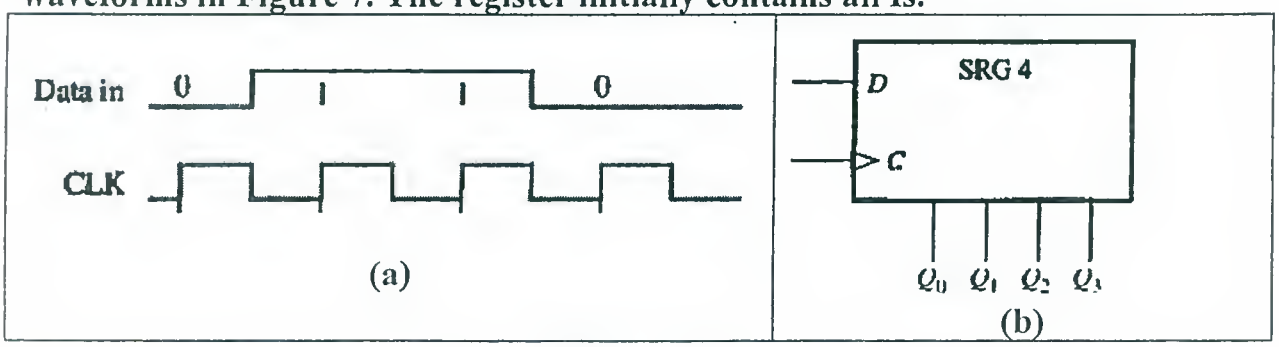


Figure (6)

Q7: Show the states of the 4-bit register (SRG 4) for the data input and clock waveforms in Figure 7. The register initially contains all Is.



Figure(7)